

8040-1022

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Hirotaka NAKANO et al.

Confirmation No. 9420

Serial No. 09/855,723

Group 2645

Filed May 16, 2001

SYSTEM OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT RE

JUL 2 1 2003

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Technology Center 2600

Sir:

In compliance with Rules 1.97 and 1.98, and in ful-fillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed sheet.

A concise explanation of the relevance of these items is that these references were cited by the European Search Report in the corresponding European Application Serial No. 01 25 0174. A copy of the European Search Report in which they were cited is attached hereto.

Respectfully submitted,

YOUNG & THOMPSON

Robert J. Patch

Attorney for Applicant Registration No. 17,355 745 South 23rd Street

Arlington, VA 22202

Telephone: 703/521-2297

July 18, 2003